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WORD OFFSET	BIT	DESCRIPTION	INITIAL SETTING BY IOP	VALUE STORED BY CHN
0	0-7	SEQUENCE NUMBER	0	SEQUENCE #
	8-15	AVAILABLE EXCHANGES	0	AVAILABLE LCs
	16-31	TOTAL QUEUED IN CHANNEL	0	TOTAL QUEUED
1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER- WISE)	0-7	CONTROL BLOCK CODE	0xFC	0xFC
	8	CONTROL BLOCK CODE QUALIFIER	0	0
	9-12	RESERVED	0	0
	13	CHN UNAVAILABLE (NOT USED)	0	0
	14	CHN ALLOWED TO STORE INTO AREA	1	1
	15	CHN DID STORE INTO AREA	0	1
	16-23	CHID	CHID	CHID
	24-31	RESERVED	0	0
	2x256	2 BITS PER PORT QUEUE COUNTERS	0	SET PER PORT
	18-31	RESERVED - FOR EITHER CHN OR IOP (JUST IN CASE)	0	DON'T STORE ANYTHING

FIG.2

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WORD OFFSET	BIT	DESCRIPTION	INITIAL SETTING BY IOP	VALUE STORED BY CHN
0	0-7	SEQUENCE NUMBER	0	SEQUENCE #
	8-15	AVAILABLE EXCHANGES	0	AVAILABLE EXCH.
	16-31	TOTAL QUEUED IN CHANNEL	0	TOTAL QUEUED
1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER- WISE)	0-7	CONTROL BLOCK CODE	0xFC	0xFC
	8	CONTROL BLOCK CODE QUALIFIER	0	0
	9-12	RESERVED	0	0
	13	CHN UNAVAILABLE (NOT USED)	0	0
	14	CHN ALLOWED TO STORE INTO AREA	1	1
	15	CHN DID STORE INTO AREA	0	1
	16-23	CHID	CHID	CHID
	24	DMA STORAGE REQUEST QUEUE THRESHOLD REACHED	0	SET TO 1 IF REACHED
	25-31	RESERVED	0	0
		RESERVED - FOR EITHER CHN OR IOP (JUST IN CASE)	0	DON'T STORE ANYTHING
2-31				

FIG.3

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WORD OFFSET	BIT	DESCRIPTION	INITIAL SETTING BY IOP	VALUE STORED BY IOP
0	0-7	SEQUENCE NUMBER	0	SEQUENCE #
	8-15	RESERVED	0	0
	16-31	TOTAL QUEUED IN CHANNEL	0	TOTAL QUEUED
1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER- WISE)	0-7	CONTROL BLOCK CODE	0xFC	0xFC
	8	RESERVED	1	1
	9-13		0	0
	14	IOP ALLOWED TO STORE INTO AREA	1	1
	15	IOP DID STORE INTO AREA	0	1
	16-23	CHID	CHID	CHID
	24-31	RESERVED	0	0
2-9	1x256	IOP_Q2BUSY	0	SET PER PORT
10-17	1x256	IOP_Q1BUSY	0	SET PER PORT
18-25	1x256	IOP_PREVQBUSY	0	SET PER PORT
26-31		RESERVED	0	0

FIG.4

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WORD OFFSET	BIT	DESCRIPTION	INITIAL SETTING BY IOP	VALUE STORED BY IOP
0	0-7	SEQUENCE NUMBER	0	SEQUENCE #
	8-15	RESERVED	0	0
	16-31	TOTAL QUEUED IN CHANNEL	0	TOTAL QUEUED
1 (IOP WILL SET FOR zSERIES ONLY! ZERO, OTHER- WISE)	0-7	CONTROL BLOCK CODE	0xFC	0xFC
	8	CONTROL BLOCK CODE QUALIFIER	1	1
	9-13	RESERVED	0	0
	14	IOP ALLOWED TO STORE INTO AREA	1	1
	15	IOP DID STORE INTO AREA	0	1
	16-23	CHID	CHID	CHID
2-31	24-31	RESERVED	0	0
		RESERVED	0	0

FIG.5

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BIT	DESCRIPTION	FCV	FC	NON-FICON
0-1			0	0
2	NUMBER OF STARTS QUEUED TO PORT -OR- BUSYNESS OF CHANNEL	CHN_QCOUNT(PORT) + IOP_Q1BUSY(PORT) + IOP_Q2BUSY(PORT) (TOTAL NUMBER OF STARTS QUEUED TO THE PORT)	FC_UMAXSTOREEQS + "AEX" NOTE: TO COMPUTE AEX: IF AVAILABLEEXCHANGES = 0, THEN "AEX" = 1. OTHERWISE, "AEX" = 0	ONE DEEP QUEUE BIT FROM VECTOR. FOR PRE-zSERIES, SET BIT TO 0
3				CHANNEL BUSY VECTOR BIT
4	LINK INIT REQ'D	IF LINK INIT REQUIRED, SET BIT TO 1		
5	PREVIOUSLY QUEUED START	IOF_PREVQBUSY(PORT)	0	0
6	DESTINATION PORT BUSY	0	0	0
7	CHANNEL HARDWARE AVAILABILITY	IF AVAILABLEEXCHANGES = 0, SET BIT TO 1. OTHERWISE, SET TO 0	"AEX" -OR'D WITH - FC_MAXSTOREEQS	CHANNEL BUSY VECTOR BIT
8-13	RESERVED	0	0	0
14	UNKNOWN PATHWEIGHT STATE	IF FICON PATH NOT STORING STATISTICS IN HSA (FC/FCV_STATSACTIVE = 0), SET THIS BIT TO 1. FOR PRE-zSERIES NON-FICON PATHS: IF PATH IS ON ANOTHER IOP -OR- THE CHANNEL BUSY VECTOR IS ON, SET THIS BIT TO 1		
15	FAVOR PREFERRED PATH	SET TO 1 IF PREFERRED PATH BIT IS ON & THIS PATH IS NOT PREFERRED PATH		
16-31	TOTAL QUEUED IN CHANNEL	FCV_TOTALQUEUED + IOP_TOTALQUEUED	FC_TOTALQUEUED + IOP_TOTALQUEUED	CHANNEL BUSY VECTOR BIT x 8

FIG.6